

CLAIMS

What is claimed is:

1 1. A method for early packet steering by examining a packet as it is received at
2 a routing location, thereby avoiding having to store the entire packet in memory
3 prior to processing, said method comprising the steps of:

4 (1) parsing the packet as it is received to thereby extract portions of a
5 packet header;

6 (2) processing the packet header in parallel before the arrival of a packet
7 payload being carried by the packet; and

8 (3) steering the packet to a correct address without storing the entire
9 packet payload in memory.

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1 2. The method as defined in claim 1 wherein the method further comprises the
2 step of collapsing a plurality of parsing decisions for the packet into a single
3 operation;

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1 3. The method as defined in claim 2 wherein the method further comprises the
2 step of simultaneously performing a plurality of compare and branch operations in a
3 single clock cycle to thereby parse a destination address of the packet.

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1 4. The method as defined in claim 3 wherein the method further comprises the
2 step of passing the packet to an output port immediately upon arrival of the packet
3 payload.

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1 5. The method as defined in claim 4 wherein the method further comprises the
2 step of parsing the packet after arrival of the initial 64 bits of the packet header of
3 the packet.

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1 6. The method as defined in claim 5 wherein the method further comprises the
2 step of determining before the first 64 bits have arrived if there is a problem with the
3 packet which will preclude further processing of the packet.

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1 7. The method as defined in claim 6 wherein the method further comprises the
2 steps of:

3 (1) receiving the packet into an elastic buffer to thereby enable the system to
4 perform its analysis before the entire packet arrives; and

5 (2) parsing information from the packet header in parallel, including
6 destination address, source address, information to perform a cyclical redundancy
7 check (CRC) and a hash table comparison, protocol analysis, and length analysis.

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1 8 The method as defined in claim 7 wherein the method further comprises the
2 step of compiling early packet steering statistics that are utilized to determine if the
3 packet is valid, and a destination address for routing the packet.

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1 9. The method as defined in claim 8 wherein the method further comprises the
2 steps of:

3 (1) treating the destination address as an index that points to a physical port;
4 and

5 (2) mapping directly to the physical port address utilizing content
6 addressable memory techniques such that rather than billions of possible outcomes,
7 a comparison is valid for a relatively small and manageable number of physical
8 ports.

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1 10. The method as defined in claim 9 wherein the method further comprises the
2 step of utilizing the source address analysis to determine if an incoming packet has
3 special requirements including special routing, special actions or rejection.

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1 11 The method as defined in claim 10 wherein the method further comprises the
2 step of performing the CRC calculation in hardware as the packet arrives, thereby
3 removing that step from a host CPU and saving overhead, wherein the CRC can be
4 performed as soon as the destination address has arrived in the packet.

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1 12. The method as defined in claim 11 wherein the method further comprises the
2 steps of:

3 (1) generating a status word, wherein the status word is utilized to transfer
4 the packet to a correct destination address; and

5 (2) appending the status word to the packet so that it can be retrieved from as
6 the packet as is necessary.

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1 13. The method as defined in claim 12 wherein the method further comprises the
2 steps of:

3 (1) storing a destination address in the status word;

- 4 (2) storing a source address in the status word;
- 5 (3) storing an alignment byte in the status word;
- 6 (4) storing a protocol field in the status word; and
- 7 (5) storing an end of packet field in the status word.

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1 14. The method as defined in claim 13 wherein the method further comprises the
2 step of reducing latency of the packet as it is received, thereby reducing a cost of the
3 system because less memory is required for storing incoming packets, and less
4 support circuitry is required to support the memory.

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1 15. The method as defined in claim 14 wherein the method further comprises the
2 steps of:

- 3 (1) reducing a total time between input and output of the packet; and
- 4 (2) reducing overhead on a system bus by parsing the packet header without
- 5 having to send the packet header to the host CPU.